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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/575,819	04/13/2006	Seong-Young Lee	AB-1867 US	5258

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EXAMINER	
HARDING, SARAH K	
ART UNIT	**PAPER NUMBER**
2814	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/575,819	LEE ET AL.	
	Examiner	Art Unit	
	Sarah K. Harding	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/13/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, &8-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Ikeda (US PGPub 2001/003023).

Ikeda teaches claim 1: A thin film transistor comprising (FIG. 1 & 9; [0004, 0013]):

a. a gate electrode (2F);

b. a gate insulating layer (3) formed on the gate electrode (2F);

c. a semiconductor layer (4) formed on the gate insulating layer (3) and disposed opposite the gate electrode (2F);

d. a source electrode (5S) and a drain electrode (5D) that are formed at least in part on the semiconductor layer(4) and face each other;

e. a passivation layer (7,9) formed on the source electrode (5S), the drain electrode (5D), and a portion of the semiconductor layer (4) that is not covered with the source electrode (5S) and the drain (5D) electrode;

f. and a shielding electrode (2R) formed on the passivation layer (7,9) and disposed on a region between the source electrode (5S) and the drain electrode (5D).

Claim 9: A thin film transistor array panel comprising (FIG. 1 & 9; [0004, 0013]):

a. a gate line (43) and a data line (44);

b. a first thin film transistor including a control electrode (2F), an input electrode (5S), an output electrode (5D), and a channel portion (Ch) disposed between the input electrode (5S) and the output electrode (5D) and generating a gate signal to be applied to the gate line (44) [0013, 0028, 0032-0034];

c. a second thin film transistor including a gate (2F) connected to the gate line (44), a source electrode (5S) connected to the data line (44), a drain electrode (5D), and a channel portion (Ch) disposed between the source electrode (5S) and the drain electrode (5D) and transmitting a data signal from the data line in response to the gate signal from the gate line [0012-0013, 0028, 0032-0034, 0039];

d. a pixel electrode (10) connected to the drain electrode (5D) to receive the data signal;

g. and a first shielding electrode (2R) disposed on the channel (Ch) portion of the first thin film transistor (FIG. 1).

Claim 19. A display device comprising (FIG. 1 & 9; [0004, 0013]):

a. a gate line (43) and a data line (44);

b. a first thin film transistor including a channel portion (Ch) and generating a gate signal to be applied to the gate line (44) [0012-0013, 0028, 0032-0034, 0039];

c. a second thin film transistor transmitting a data signal from the data line in response to the gate signal from the gate line (44) [0012-0013, 0028, 0032-0034, 0039];

d. a pixel electrode (10) connected to the second thin film transistor to receive the data signal) [0012-0013, 0028, 0032-0034, 0039];

e. a shielding electrode (2R) disposed on the channel portion (Ch) of the first thin film transistor;

f. and a common (opposite) electrode facing the pixel electrode (10) [0039] (Fig. 9).

Claims 2 & 10: Ikeda teaches the shielding electrode (2R) is electrically isolated (by 7) (FIG. 1; [0013]).

Claims 3 & 11: Ikeda teaches the shielding electrode (2R) is supplied with a predetermined voltage [0012, 0028, 0032-0034].

Claims 4 & 12: Ikeda teaches the predetermined voltage supplied to the shielding electrode is equal to or lower than a ground voltage [0012, 0028, 0032-0034].

Claims 5 & 13: Ikeda teaches the predetermined voltage supplied to the shielding electrode is a negative voltage [0012, 0028, 0032-0034].

Claims 8 & 18: Ikeda teaches the passivation/ insulating layer comprises organic insulator [0030].

Claims 14 & 22: Ikeda teaches the predetermined voltage supplied to the first shielding electrode has a magnitude for turning off the second thin film transistor [0012, 0028, 0032-0034].

Claims 15 & 23: Ikeda teaches the first shielding electrode (2R) comprises the same layer as the pixel electrode (10).

Claim 16: Ikeda teaches a second shielding electrode disposed (2R) on the channel portions (Ch) of the second thin film transistor and including the same layer as the pixel electrode (10) ([0012] Fig. 9).

Claim 17: Ikeda teaches an insulating layer (7,9) disposed between the first and the second thin film transistors (2F) and the first and the second shielding electrodes (2R).

Claim 20: Ikeda teaches the shielding electrode (2R) faces the common (opposite) electrode [0039].

Claim 21. The display device of claim 20, wherein the shielding electrode is supplied with a predetermined voltage lower than a voltage applied to the common electrode.

Claim 24: Ikeda teaches a dielectric layer (17) disposed between the shielding electrode (2R) and the common electrode [0039].

Claim 25: Ikeda teaches the dielectric layer (17) comprises a liquid crystal layer [0039].

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda (US PGPub 2001/003023) as applied to claim 1 above, and further in view of Yanagawa et al. (US PGPub 2001/0038432)

Regarding claim 6, as described above, Ikeda substantially reads on the invention as claimed, except Ikeda does not teach the shielding electrode comprises ITO. Yanagawa teaches the shielding electrode comprises ITO so that it is transparent allowing the light to transmit thought the electrode to the pixel area [0107]. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the shield electrode taught by Ikeda to be made of ITO so that its transparency does not block the transmission of light onto the pixel area as taught by Yanagawa [0107].

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda (US PGPub 2001/003023) as applied to claim 1 above, and further in view of Tsubo (US PGPub 2002/0057396)

Regarding claim 7, as described above, Ikeda substantially reads on the invention as claimed, except Ikeda does not teach the shielding electrode has a shape of horseshoes. Tsubo teaches a U-shape shielding electrode which reduces the

variance in parasitic capacitance of the device [0061, 0072]. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the shield electrode taught by Ikeda to be a U-shape to increase the performance of the device as taught by Tsubo [0061, 0072].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sarah K. Harding whose telephone number is (571) 270-1266. The examiner can normally be reached on M-R 7:30-5:00pm every other F 7:30-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SKH
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THERESA DOAN
PRIMARY PATENT EXAMINER